AMENDMENTS TO THE CLAIMS

1) (Currently amended) A ~~sputtered silicon~~ micro-machined structure ~~being positioned on a work piece together with~~ comprising:

a structural layer consisting essentially of sputtered silicon, said structural layer comprising a core silicon layer; and

a pre-fabricated integrated electronic circuitry electrically coupled to said structural layer, said pre-fabricated integrated electronic circuitry is characterized as an operational semiconductor circuitry ~~and being formed on top of a sacrificial layer, said sputtered silicon structure having a thermal fabrication budget, said operational circuitry having a first critical thermal budget, wherein said thermal fabrication budget~~ is ~~smaller than said first critical thermal budget~~.

2) (Currently amended) ~~A sputtered silicon~~ The micro-machined structure ~~being formed on top~~ of ~~a sacrificial layer~~ claim 1, wherein said ~~sputtered silicon structure having a thermal fabrication budget, said sacrificial~~ structural layer ~~having a second critical thermal budget, wherein said thermal fabrication budget is smaller than said second critical thermal budget~~ further comprises:

at least one conductive layer in contact with said core silicon layer.

3) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~1~~2, wherein said ~~sacrificial~~ at least one conductive layer is made from a Titanium based material ~~dissolvable by a wet etchant~~.

4) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~3~~2, wherein said ~~wet etchant~~ at least one conductive layer is made from a material selected from a group consisting of ~~6:1-20:1 buffered HF and $NH_4HF+HC_2H_3O_2+H_2O$~~ TiW and TiN.

5) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~4 having a first permeability rate that is up to ten times higher than a second wet etchant permeability rate of a comparable polysilicon structure~~ 2, in which said core silicon layer and said at least one conductive layer have essentially the same shape.

6) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~1 or~~ 2, wherein

said ~~sacrificial~~ core silicon layer ~~is made from a material dissolvable by a dry etchant~~ has a first dissolving characteristic and said at least one conductive layer has a second dissolving characteristic and wherein said second dissolving characteristic is compatible with said first dissolving characteristic.

7) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~6~~1, wherein said ~~material is an organic material~~ operational semiconductor circuitry includes an aluminum-based metalization.

8) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~7~~1, wherein said ~~organic material~~ operational semiconductor circuitry is ~~polyimide~~ a complimentary metal oxide semiconductor (CMOS) circuitry.

9) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim 1 ~~or 2~~, ~~wherein said sputtered silicon structure comprises a post-annealing configuration resulting from a pre-annealing configuration and a low temperature annealing transformation~~ further comprising:

at least one sealing layer.

10) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~1~~9, wherein said ~~operational semiconductor circuitry includes an aluminum metalization~~ at least one sealing layer consisting essentially of silicon nitride.

11) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~10~~1, wherein

said ~~thermal fabrication budget~~ core silicon layer is ~~provided by a maximum annealing temperature of not more than 450° C~~ made from boron doped silicon.

12) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim 1 ~~or 2 being a released structure~~, wherein

said core silicon layer is made from silicon doped with 40-80 ppm boron.

13) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~12~~1, wherein

said ~~released~~ micro-machined structure ~~has~~ is characterized as having an essentially buckling-free deformation configuration.

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14) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~13 resulting from a sputtering with first sputtering criteria including:~~

~~A) an etchant selection; and~~

~~B) a sputtered structure thickness~~ 1, wherein

said core silicon layer has a predetermined thickness which influences a strain gradient of said micro-machined structure.

15) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~14~~1, wherein said ~~etchant selection is made from a group consisting of 6:20:1 buffered HF and $NH_4HF+HC_2H_3O_2+H_2O$~~structural layer further comprises:

a first conductive layer in contact with and on top of said core silicon layer; and

a second conductive layer in contact with and below said core silicon layer, wherein said first and second conductive layers have essentially the same shape as said core silicon layer.

16) (Currently amended) The ~~sputtered silicon~~ micro-machined structure of claim ~~13~~1, wherein

said micro-machined structure is characterized as having a variable sputtered layer thickness and a correlated curvature, wherein said correlated curvature essentially decreases with an increase of the variable sputtered layer thickness.

Claims 17-41 (Cancelled).